wherein the semiconductor device is adhered to the substrate with the bonding material which is positioned between adjacent ones of the plurality of vacant spaces.

REMARKS

Claims 1-4, and 6-24 are now pending in the application. The amendments to the claims contained herein are of equivalent scope as originally filed and, thus, are not a narrowing amendment. The Examiner is respectfully requested to reconsider and withdraw the rejections in view of the amendments and remarks contained herein.

REJECTION UNDER 35 U.S.C. § 102

Claims 1, 8, 18, and 24 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Yamazaki (JP 02-133936). This rejection is respectfully traversed.

Yamazaki discloses a gap material that acts as a "spacer" to disperse stress uniformly over the whole semiconductor element. The Examiner alleges that this gap material occupies a space within the bonding layer such that there are areas where there is no bonding material, and therefore, anticipates the claimed space. Applicant respectfully asserts, however, that the amended claims are not anticipated by Yamazaki.

The claims have been amended to call for the spaces in the bonding layer to be vacant spaces, which is supported by the drawings of the application as originally filed. As Yamazaki discloses a gap material acting as spacers in the bonding layer, the claimed vacant space is not anticipated.

Claim 9 stands rejected under 35 U.S.C. § 102(b) as being anticipated by Takeshi (EP 0 517 071). This rejection is respectfully traversed.

Claim 9 has been amended and rewritten. More specifically, claim 9 now calls for a semiconductor device connecting method for connecting a semiconductor device onto a substrate wherein the bonding layer is pressurized to a pressure in the range of 12 kgf to 20 kgf and heated to a temperature in the range of 260°C to 360°C. Claim 9 now also calls for the plurality of vacant spaces to be formed by decreasing the viscosity of a bonding material to cause the bonding material to flow outward from the semiconductor device and controlling the formation of the plurality of vacant spaces such that a percentage of the vacant spaces in the bonding layer is 5% to 70%.

Takeshi does not anticipate the above claims. Rather, Takeshi only discloses applying an IC chip to a flexible board with heat and pressure. There is no disclosure of particular pressures or temperatures for such a process.

Furthermore Takeshi, in columns 1-2, lines 56-58 and 1-3, discloses that when the adhesive is heated bubbles may be produced from the adhesive between the flexible board and IC chip. One skilled in the art readily appreciate that when the adhesive of Takeshi is heated, a gas is evolved from the adhesive that causes bubbles. This contrasts with the claimed method of claim 9.

Claim 9 calls for forming a plurality of vacant spaces by decreasing the viscosity of the bonding material. This decrease in the viscosity of the bonding material causes the bonding material to flow outward. As the bonding material flows outward, vacant spaces are formed. By utilizing such a method, one can control the percentage of vacant spaces produced (i.e., 5 – 70% as claimed). Takeshi discloses that bubbles

made of chemical gas or air are released by heating the adhesive. This is different from reducing the viscosity such that the bonding material flows outward to leave vacant spaces. As such, the claimed method is not anticipated. Therefore, reconsideration and withdrawal of this rejection is respectfully requested.

REJECTION UNDER 35 U.S.C. § 103

Claims 2-7, 10, and 21 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yamazaki (JP 02-133936) as applied to claims 1 and 9 and further in view of Muramatsu (U.S. Pat. No. 5,893,623). This rejection is respectfully traversed.

Applicant respectfully asserts that these dependent claims should be in condition for allowance for at least the same reasons as the independent base claims. More particularly, Yamazaki does not disclose a vacant space present in the bonding layer. Yamazaki discloses spacers in the form of a gap material. As such, these dependent claims are not obvious.

Furthermore, it would not have been obvious to use the epoxy resin of Muramatsu for at least the same reasons.

Claims 11-17, 19, 20, 22, and 23 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Applicant's admitted prior art (APA) in view of Yamazaki (JP 02-133936). This rejection is respectfully traversed.

The Examiner alleges that the admitted prior art does not show a plurality of spaces formed within a bonding layer, but Yamazaki utilizes spaces close to each other within a bond layer. The Examiner also alleges that it would have been obvious to form spaces in the bond layer to disperse internal stress as taught by Yamazaki.

As described above, Yamazaki does not disclose a vacant space but teaches spacers in the form of a gap material. Yamazaki contains no suggestion or motivation to employ a plurality of vacant spaces to disperse internal stress. Absent this motivation, the claims would not have been obvious.

Furthermore, the Examiner alleges that it would have been obvious to one of ordinary skill in the art to form the percentage of spaces within the bonding layer from 5% to 70% because optimum or working ranges involve only routine skill in the art. Applicant respectfully asserts, however, that none of the references cited provide any motivation or suggestion to form vacant spaces within such a range. Moreover, Applicant respectfully asserts that the cited references actually teach away from the use of vacant spaces wherein a percentage of the vacant spaces is between 5% - 70%.

More particularly, as stated above, Yamazaki teaches forming spacers in the form of a gap material. Teaching the use of a gap material to disperse stress completely teaches away from the use of a vacant space to absorb deformation of the semiconductor device or substrate.

Takeshi also directly teaches away from this aspect of the claims. Takeshi teaches that when an adhesive is heated, bubbles of chemical gas or air are released from the adhesive. Takeshi further teaches, however, that, "When the bubble 8 remains between the flexible board 1 and the IC chip 3, the bubble 8 is expanded and contracted in response to the change of temperature, thereby causing the interconnection portion to be cracked or peeled off. As a result, reliability of the interconnection is deteriorated." (column 2, lines 9-15). This contrasts with the teachings of the claimed invention. The claimed invention utilizes the vacant spaces in order to absorb deformation and to

enable a reliable connection between the semiconductor device and the substrate (page 7, lines 5-16).

Takeshi further teaches that it is an object of his invention to provide a chip device bonding machine which can effectively prevent bubbles from remaining in the adhesive between a flexible board and an IC chip (column 2, lines 30-34). Takeshi, therefore, teaches that these bubbles are not desirable and further teaches a method of eliminating them. As such, Takeshi directly teaches away from a semiconductor connecting structure and a semiconductor connecting method that utilizes vacant spaces in a range of 5%-70% as claimed.

By directly teaching away from the claimed invention, the claimed range of 5%-70% would not have been obvious in view of Yamazaki or Takeshi and, therefore, reconsideration and withdrawal of this rejection is respectfully requested.

CONCLUSION

It is believed that all of the stated grounds of rejection have been properly traversed, accommodated, or rendered moot. Applicant therefore respectfully requests that the Examiner reconsider and withdraw all presently outstanding rejections. It is believed that a full and complete response has been made to the outstanding Office Action, and as such, the present application is in condition for allowance. Thus, prompt and favorable consideration of this amendment is respectfully requested. If the Examiner believes that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at (248) 641-1600.

Respectfully submitted,

Dated: _____

By: _____
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ATTACHMENT FOR CLAIM AMENDMENTS

The following is a marked up version of each amended claim in which underlines indicates insertions and brackets indicate deletions.

1. (Twice Amended) A semiconductor device connecting structure for connecting a semiconductor device onto a substrate, characterized by comprising:

a bonding layer interposed between said semiconductor device and said substrate to accomplish adhesion therebetween, which includes a bonding material for adhering said semiconductor device onto said substrate and a plurality of vacant spaces formed within said bonding material,

wherein a percentage of said plurality of vacant spaces within said bonding material is 5% to 70%.

3. (Thrice Amended) A semiconductor device connecting structure as defined in claim 1, characterized in that said plurality of vacant spaces are placed closely to each other.

5. (Thrice Amended) A semiconductor device connecting structure as defined in claim 1, characterized in that the percentage of said plurality of vacant spaces within said bonding material is 5% to 70%.

6. (Thrice Amended) A semiconductor device connecting structure as defined in claim 5, characterized in that the percentage of said plurality of vacant spaces within said bonding material is 10% to 30%.

9. (Twice Amended) A semiconductor device connecting method for connecting a semiconductor device onto a substrate, characterized by comprising the steps of:

interposing a bonding layer between said semiconductor device and said substrate to accomplish adhesion therebetween;

joining said substrate and said semiconductor device to each other by pressing a pressurizing head[, heated up to a high temperature,] against said semiconductor device to pressurize [and heat] said bonding layer to a pressure in a range of 12 kgf to 20 kgf; [and]

heating said pressurizing head to a temperature in a range of 260°C to 360°C in order to heat said bonding layer;

forming a plurality of vacant spaces within said bonding layer by decreasing a viscosity of a bonding material of said bonding layer to cause said bonding layer to flow outward from said semiconductor device; and

controlling the formation of said plurality of vacant spaces to provide a percentage of said plurality of vacant spaces within said bonding material in a range of 5% to 70%.

11. (Twice Amended) A liquid crystal display unit comprising:

a pair of liquid crystal holding substrates disposed in an opposed relation to each other with liquid crystal therebetween;

a semiconductor device connected onto at least one of said liquid crystal holding substrate; and

a bonding layer interposed between said liquid crystal holding substrate and said semiconductor device to accomplish adhesion therebetween, characterized in that

said bonding layer includes a bonding material for adhering said semiconductor device onto said liquid crystal holding substrate and a plurality of vacant [spacers] spaces formed within said bonding material.

13. (Thrice Amended) A liquid crystal display unit as defined in claim 11, characterized in that said plurality of vacant spaces are placed closely to each other.

15. (Thrice Amended) A liquid crystal display unit as defined in claim 11, characterized in that the percentage of said plurality of vacant spaces within said bonding material is 5% to 70%.

16. (Thrice Amended) A liquid crystal display unit as defined in claim 15, characterized in that the percentage of said plurality of vacant spaces within said bonding material is 10% to 30%.

17. (Twice Amended) An electronic apparatus having a plurality of semiconductor driving output terminals and a liquid crystal display unit connected to said semiconductor driving output terminals, characterized in that said liquid crystal display unit includes:

a pair of liquid crystal holding substrates disposed in an opposed relation to each other with liquid crystal therebetween;

a semiconductor device connected onto at least one of said liquid crystal holding substrates; and

a bonding layer interposed between said liquid crystal holding substrate and said semiconductor device to accomplish adhesion therebetween,

wherein said bonding layer includes a bonding material for adhering said semiconductor device onto said liquid crystal holding substrate and a plurality of vacant spaces formed within said bonding material.

18. (Amended) A semiconductor device connecting structure comprising:

a substrate;

a semiconductor device connected to the substrate; and

a bonding layer interposed between the substrate and the semiconductor device, the bonding layer including a bonding material adhering the semiconductor device to the substrate, a plurality of conductive particles dispersed in the bonding material, and a plurality of vacant spaces formed within said bonding material,

wherein the semiconductor device is adhered to the substrate by the bonding material at a substantially plane center portion of the semiconductor device.

19. (Amended) A liquid crystal display comprising:

a substrate;

a liquid crystal on the substrate;

a plurality of electrodes on the substrate;

a semiconductor device having a plurality of bumps, the semiconductor device being mounted on the substrate, each bump being connected to one of said plurality of electrodes;

a bonding layer interposed between the substrate and the semiconductor device, the bonding layer including a bonding material adhering the semiconductor device to the substrate, and a plurality of vacant spaces formed within said bonding material,

wherein the plurality of vacant spaces are at least formed in an area encompassed by the plurality of electrodes.

20. (Amended) A liquid crystal display comprising:

a substrate;

a liquid crystal on the substrate;

a semiconductor device mounted on the substrate, the semiconductor device including a periphery defining a mounting area;

a bonding layer interposed between the substrate and the semiconductor device, the bonding layer including a bonding material adhering the semiconductor

device to the substrate, and a plurality of vacant spaces formed within said bonding material,

wherein the plurality of vacant spaces are at least formed in the mounting area.

21. (Amended) A liquid crystal display according to claim [3] 20, wherein a region occupied by the bonding layer is larger than the mounting area.

22. (Amended) A liquid crystal display comprising:

a substrate;

a liquid crystal on the substrate;

a plurality of electrodes on the substrate;

a semiconductor device having at least two edges opposing each other, and a plurality of bumps aligned along at least said two edges,

the semiconductor device being mounted on the substrate, each bump being connected to an electrode;

a bonding layer interposed between the substrate and the semiconductor device, the bonding layer including a bonding material adhering the semiconductor device to the substrate, and a plurality of vacant spaces formed within said bonding material,

wherein the vacant spaces are at least formed in an area bordered by the electrodes.

23. (Amended) A liquid crystal display comprising:

a first substrate;

a second substrate including an overlapping area overlapping the first substrate;

a plurality of electrodes formed on the first substrate, each of the plurality of electrodes at least extending toward the overlapping area;

a semiconductor device having a plurality of bumps, the semiconductor device being mounted on the substrate, each bump being connected to one of the plurality of electrodes;

a bonding layer interposed between the substrate and the semiconductor device, the bonding layer including a bonding material adhering the semiconductor device to the substrate, and a plurality of vacant spaces formed within said bonding material,

wherein the plurality of vacant spaces are at least formed in an area encompassed by the bumps.

24. (Amended) A semiconductor device connecting structure comprising:

a substrate;

a semiconductor device connected to the substrate; and

a bonding layer including a bonding material that joins the semiconductor to the substrate and a plurality of spaces disposed in the bonding material, the bonding layer being disposed between the substrate and the semiconductor device,

wherein the semiconductor device is adhered to the substrate with the bonding material which is positioned between adjacent ones of the plurality of vacant spaces.